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Notice of Allowability	Application No.	Applicant(s)	
	10/643,876	HUANG ET AL.	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amdt on August 22, 2005*.

2. ☒ The allowed claim(s) is/are *1 - 4*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

DETAILED ACTION

Response to Amendment

1. This office action is in response to Amendment filed on August 22, 2005

2. Claims **1 – 4** have been amended.

3. Claims **1 – 4** are presented for examination.

Drawings

4. The drawings were received on August 22, 2005. These drawings are acceptable.

EXAMINER'S AMENDMENT

5. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Allen Wood on October 20, 2005 and on October 25, 2005.

The application has been amended as follows:

Claim 1:

-- 1. (currently amended) A layout of a flash memory having a plurality of symmetric select transistors, comprising:

a memory cell array;

polysilicon gates of the plurality of symmetric select transistors extending in a direction perpendicular to a side of the memory cell array and cooperating with a plurality of pairs of sources/drains for forming the plurality of symmetric select transistors; and

wires connecting the plurality of symmetric select transistors and the memory cell array. --

Claim 3:

-- 3. (currently amended) A layout of a flash memory having a plurality of symmetric select transistors, comprising:

a memory cell array; and

polysilicon gates corresponding to the plurality of symmetric select transistors extending in a direction perpendicular to a side of the memory cell array;

wherein the plurality of symmetric select transistors are arranged substantially symmetric with respect to the side of the memory cell array. –

Claim 4:

-- 4. (currently amended) The layout according to claim 3, further comprising a metal wires extending from the memory cell array toward the polysilicon gates for connecting the plurality of symmetric select transistors to the memory cell array. --

Allowable Subject Matter

6. Claims **1 – 4** are allowed.

7. The following is an examiner's statement of reasons for allowance: Claims **1 – 4** are allowable over the prior art of record because none of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach:

polysilicon gates of a plurality of symmetric select transistors extending in a direction perpendicular to a side of the memory cell array as cited in the independent claims 1 and 3; and among other limitations as cited in the independent claims 1 and 3.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Tran LT

October 26, 2005

David Nelms
Supervisory Patent Examiner
Technology Center 2800